San José State University
Computer Science Department
CS247, Advanced Computer Architecture, Section 1, Spring 2023

Course and Contact Information

Instructor: Robert Chun

Office Location: MH 413 (also, On-Line)

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Office Hours: MW 1:30pm-2:30pm (and by appointment, On-Line)

Class Days/Time: MW 4:30pm - 5:45pm

Classroom: MH 422

Prerequisites: CS147 (Introductory Course in Comp. Architecture), also Operating Systems

Faculty Web Page

Course materials such as presentation slides, notes, assignments, etc. can be found on my faculty web page at http://www.sjsu.edu/people/Robert.Chun/courses

Course Description

Detailed analysis of high-performance, fault-tolerant computer systems. Survey various machine architectures including implementation alternatives for major processor sub-systems. Pipelined, vector, VLSI, multi-core and dataflow architectures are examined. Discussion includes data representation, arithmetic logic unit operations and algorithms, rounding algorithms, control unit operation and instruction formats. Performance measurement and speedup techniques are studied to perform tradeoff analysis and design optimization. Digital breadboard labs and programming projects with the VHDL language and simulation environment will be used to demonstrate computer-aided design and functional verification techniques for digital systems. A written report and oral presentation on a relevant and approved topic of interest to the student will be required.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- Understand combinatorial and sequential circuit structures and Boolean number representation schemes
- Appreciate how the fundamental core mathematical operations such as addition, subtraction, multiplication, and division can be optimized with appropriate number representation, rounding, and digital circuit implementation schemes.
- Explain the tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- Discuss non-classical architectures such as parallel processors, multi-core chips, pipelined and VLIW machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- Emphasize the importance of fault-tolerant design techniques and examine various methods of error detection and correction such as TMR and Hamming Codes.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Utilize computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- Use industrial-grade field programmable gate array chips and their associated CAD toolsets.
- Appreciate how hardware and software (especially the operating system and compilers) must work synergistically together to provide optimum throughput.
- Perform an in-depth investigation of an architecture related topic of interest to them and present their findings to their classmates in an oral and written report using a venue similar to that used in formal professional technical conferences.

Required Texts/Readings

Textbooks

Computer Organization and Design: The Hardware/Software Interface, 4th Ed., Revised Printing, D. Patterson, 2009, Morgan Kaufmann, ISBN 9780123744937

A VHDL Primer, J. Bhasker, 3rd Ed., 1999, Prentice Hall, ISBN 9780130965752

CS 247 Course Reader, Chun. Instructor will distribute to all enrolled students.

Course Requirements and Assignments

Assignments include two midterms, one final, a written and oral Term Paper/Project report, a set of homework projects (consisting of a combination of written problems and VHDL programming assignments), and active participation during student presentations, weighted as shown below. Grading is based on a class curve. All assignments (especially the oral presentation) must be completed by the student on the due date specified in order to receive credit for the class. Late assignments (including the scheduled oral presentations) or exams are not accepted and will be graded as 0 (zero) points earned. All students must uphold academic honesty, especially for the required term paper, per university policy detailed at this official SJSU website:
http://www.sjsu.edu/specialed/docs/current-forms/AcademicIntegrityPolicy.pdf

Final Examination

The final exam for the class will be held on Wednesday, May 17, 2023 2:45pm-5:00pm.

Grading Information

Assignments include two midterms, one final, a written and oral Term Paper/Project report, a set of homework projects (consisting of a combination of written problems and VHDL programming assignments), and active participation during student presentations, weighted as shown below. Grading is based on a class curve. All assignments (especially the oral presentation) must be completed by the student on the due date specified in order to receive credit for the class. Late assignments (including the scheduled oral presentations) or exams are not accepted. Any use of AI-generated text or code (e.g., via ChatGPT) is strictly forbidden and will result in a score of 0 (zero) for the assignment. All students must uphold academic honesty, especially for the required term paper, per university policy detailed at this SJSU website: http://www.sjsu.edu/specialed/docs/current-forms/AcademicIntegrityPolicy.pdf

15%	Midterm Exam 1 Approximately beginning of March
15%	Midterm Exam 2 Approximately beginning of April
30%	Written Term Paper/Project (15%) & Oral Presentations (15%) Mid-April for Written Report; Due date for Oral Presentation to be specified per student
30%	Final Exam Wednesday, May 17, 2023 2:45pm-5:00pm.
10%	Combined total of Three HW and VHDL Projects HW Projects will be due immediately before each exam

A plus = 100 to 97.0 points
A = 96.9 to 93 points
A minus = 92.9 to 90.0 points
B plus = 89.9 to 87.0 points
B = 86.9 to 82.0 points
B minus = 81.9 to 80.0 points
C plus = 79.9 to 77.0 points
C = 76.9 to 72.0 points
C minus = 71.9 to 70.0 points
D plus = 69.9 to 67.0 points
D = 66.9 to 62.0 points
D minus = 61.9 to 60.0 points
F = 59.9 points or lower

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

CS247 Spring 2023 Tentative Course Schedule

Lecture	Chapter	Topic
1-4	1, 2	Introduction, VHDL
5-6	3	Data Representation
7-10	3	High Speed Computer Arithmetic
11	Notes	Rounding
Midterm 1		*Approximately early March*
12-16	6	Pipeline and Parallel Processing
17-21	Notes	Fault-Tolerance
Midterm 2		*Approximately early April*
22-27		Term Papers & Oral Presentations
Final Exam		*Wednesday, May 17, 2023 at 2:45pm-5:00pm*

General University Policies

DISABILITIES:

If you need course adaptations or accommodations because of a disability, or if you need special arrangements in case the building must be evacuated, please inform the instructor as soon as possible. Presidential Directive 97-03 requires that students with disabilities register with DRC to establish a record of their disability.

ACADEMIC INTEGRITY:

Academic integrity is essential to the mission of San José State University. As such, students are expected to perform their own work (except when collaboration is expressly permitted by the course instructor) without the use of any outside resources. Students are not permitted to use old tests or quizzes when preparing for exams, nor may they consult with students who have already taken the exam. When practiced, academic integrity ensures that all students are fairly graded.

We all share the obligation to maintain an environment which practices academic integrity. Violations to the Academic Integrity Policy undermine the educational process and will not be tolerated. It also demonstrates a lack of respect for oneself, fellow students and the course instructor, and can ruin the university's reputation and the value of the degrees it offers. Violators of the Academic Integrity Policy will be subject to failing this course and being reported to the Office of Judicial Affairs for disciplinary action which could result in suspension or expulsion from San José State University.

CHEATING:

At SJSU, cheating is the act of obtaining or attempting to obtain credit for academic work through the use of any dishonest, deceptive, or fraudulent means. Cheating at SJSU includes but is not limited to:

Copying in part or in whole, from another's test or other evaluation instrument; Submitting work previously graded in another course unless this has been approved by the course instructor or by departmental policy. Submitting work simultaneously presented in two courses, unless this has been approved by both course instructors or by departmental policy. Altering or interfering with grading or grading instructions; Sitting for an examination by a surrogate, or as a surrogate; any other act committed by a student in the course of his or her academic work which defrauds or misrepresents, including aiding or abetting in any of the actions defined above.

PLAGIARISM:

At SJSU plagiarism is the act of representing the work of another as one's own (without giving appropriate credit) regardless of how that work was obtained, and submitting it to fulfill academic requirements. Plagiarism at SJSU includes but is not limited to:

The act of incorporating the ideas, words, sentences, paragraphs, or parts thereof, or the specific substances of another's work, without giving appropriate credit, and representing the product as one's own work; and representing another's artistic/scholarly works such as musical compositions, computer programs, photographs, painting, drawing, sculptures, or similar works as one's own.

Additional Information:

http://www.cs.sjsu.edu/greensheetinfo/index.html