San José State University

Science/Computer Science
CS 147, Computer Architecture, Section 1, FALL 2026

People

Instructor	Sriram Rao
Grader	Isaiah Mak
Peer Connections Liason	Nu Hanh Nguyen Nguyen

Course and Instructor Contact Information

Instructor:	Sriram Rao
Office Location:	DH 282
Telephone:	
Email:	sriram.rao@sjsu.edu
Office Hours:	Tuesdays 12-1 and by appointment.
Class Days/Time:	Tue/Thu: 1:30-2:45p
Classroom:	MacQuarrie Hall 224
Prerequisites:	CS 47 or CMPE 102 or equivalent (with a grade of C-" or better).

Grader and Labs Information

Labs will be published here (https://github.com/sriramsrao/CS_147_FA_26_Handouts) .

Grader	Isaiah Mak
Discord Handle	ShinyRayquay
Email	isaiah.mak@sjsu.edu
Lab Hours	
Lab Location	Discord Zoom if needed In-person on appointment
Office Hours	Thursdays, 10:00am-11:00am (official time, weekly announcement if changed)
Class Discord	**Discord Link (https://discord.gg/JdrUpAmG8)**

Labs will require the following in order to function:

- Docker
- Github account (For getting the labs.)
- **Lab Files (https://github.com/sriramsrao/CS_147_FA_26_Handouts)**

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLO)

Computer architecture is the science and art of selecting and interconnecting hardware components to create a computer that meets functional, performance and cost goals. In this course, students will learn how to completely design a correct single processor computer,

including processor datapath, processor control, memory systems, and I/O.

It describes how computers operate at a fairly low level of abstraction. For example:

- What are the components of a computer and how do they fit together?
- How do computers do arithmetic?
- Understand the functionality and operation of the basic elements of a computer system including processor, memory and input/output
- Reason about first-order performance
- Understand the hardware/software interface.
- Understand MIPS processor design as it relates to the MIPS ISA.
- Understand and design components for a single processor in Verilog.

Understanding these fundamentals thoroughly is absolutely essential to your future success in computer science. The material of this course is quite detailed and requires careful and diligent study.

Upon successfully completing this course, students will have strong systems foundation about how microprocessors are designed and how they execute programs on a single computer.

Course Requirements and Assignments

Please see **Syllabus (https://sjsu.instructure.com/courses/1635878/assignments/syllabus)**

The **University Policy S16-9 (http://www.sjsu.edu/senate/docs/S16-9.pdf)** , Course Syllabi (http://www.sjsu.edu/senate/docs/S16-9.pdf) requires the following language to be included in the syllabus:

“Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus.”

Grading Information

Please see **Syllabus. (https://sjsu.instructure.com/courses/1635878/assignments/syllabus)**

Classroom Protocol

This is your class. Please ask questions. Please come prepared. Do not engage in activity that

may distract other students.

I do not take attendance except for the first two classes. Students not attending either of the first two classes will be dropped to make room for students on the waiting list. Attempting to get marked as present (by have someone else attend in your place or using technological deceptions) will be considered academic dishonesty and at a minimum will result in you getting dropped from the course.

We will use discord channel/canvas discussion for announcements about programming labs as well as discussion topics. For faster turnarounds, please use the discord channel.

Check canvas on a weekly basis for schedules/reading assignments/due dates.

Course material developed by the instructor is the intellectual property of the instructor. Students ***should not*** publicly share or upload instructor generated material for this course such as exam questions, lecture notes, hands-on exercises or homework solutions without instructor permission.

The schedule listed in the syllabus is tentative and may change based on student needs.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' **Syllabus Information web page** **(http://www.sjsu.edu/gup/syllabusinfo/)** at http://www.sjsu.edu/gup/syllabusinfo/" Make sure to review these policies and resources.

Cheating/Academic Dishonesty

I take issues of Academic Dishonesty very seriously. ***Do not cheat***. ***Do not share code***. If we detect cheating in a programming assignment or an exam, you will get a **0** for that lab/exam. Repeat offense will likely lead to a **F** grade in the course.

All exams will be in-class. You are not allowed to use any phones during the exam.

Artificial intelligence (AI) tools like ChatGPT, Google Gemini, and GitHub Copilot are not permitted to be used as a replacement for the writing or problem-solving components of this class. SJSU's subscription to Turnitin has an AI-detection feature, and assignments that have been determined by that application or by other convincing evidence to have been written by AI in substantial fractions will receive an automatic zero. The incident will also be reported to the University as academic misconduct.

If we detect that you used AI tools for the projects, your final course grade will drop by one letter grade from whatever you would have got.

Acknowledgements

This course adapts (and also uses) materials from courses taught by Karu Sankaralingam, David Sinclair, and David Black-Schaffer. They have been adapted and modified by us with permission. As such please do not post any materials from this course on public websites.

The lecture slides for this course uses figures from the course textbook. The figures were provided by Elsevier Inc and are being distributed with permission. We are thankful for their support.

Course Syllabus

Edit

Science/Computer Science

CS 147-01, Computer Architecture, FALL 2026

Required Texts/Readings

Textbook

The **required** text book for this class is **Computer Organization and Design MIPS Edition: The Hardware/Software Interface, 6th Edition (https://www.amazon.com/dp/0128201096?ref=ppx_yo2ov_dt_b_fed_asin_title)**. We will refer to this book as H&P in the schedule below.

Online materials from the textbook publisher is available **here (https://shop.elsevier.com/books/book-companion/9780128201091)**. This contains materials from the Appendix and other content marked as "online" in the textbook.

Optional Reading

- Shing Kong, Revised by Milo Martin, The Elements of Logic Design Style
  Online: **http://www.cis.upenn.edu/~milom/elements-of-logic-design-style/ (http://www.cis.upenn.edu/~milom/elements-of-logic-design-style/)**
- Building a functional processor for the RISC-V ISA: **Pedagogically Motivated and Composable Open-Source RISC-V Processors for Computer Science Education (https://arxiv.org/pdf/2509.20514v1)**

References for Verilog

- **Verilog Cheat Sheet (https://pages.cs.wisc.edu/~karu/courses/cs552/spring2021//handouts/misc/Verilog_cheat.pdf)**

Reading

To get the most out of this class, ***prior to each lecture***, students are encouraged to read the relevant chapter from the textbook.

Other technology requirements / equipment / material

Programming assignments will be a significant part of this course. We will build programs and use run them on Linux (such as, Ubuntu 22.04). Hence, access to a computer that runs Linux will be required.

Course Requirements and Assignments

I do not grade on a curve. The exams and projects measure what you are expected to have learned.

Course Project: There will be an individual course project which entails a complete functional design of a microprocessor. All components of your design will be written in Verilog.

Programming Labs: We will be doing **individual** programming assignments**. Individual programming assignments are not group projects.** If students get help on assignments, even to resolve a seemingly trivial problem, it must be documented in the code with the name of the person rendering the help and a brief description of the help provided. Extensive help on a project will result in a reduced grade. Failure to document help, or any other forms of cheating will result in a failing grade on the assignment at a minimum and may result in failure of the course. See **Integrity (http://info.sjsu.edu/static/schedules/integrity.html)** for more information. Even in open source, you cannot copy code from one open source project to another without attribution.

Programming assignments will be distributed via Github. Please create a Github account (if you don't already have one). We will use Gradescope for assignment submission and grading.

Help on Labs: Isaiah Mak (course grader) will have weekly **online** "**lab hours (https://sjsu.instructure.com/courses/1595954)** " on Discord to help you with the labs. Please seek his help whenever needed. If in-person is necessary, please schedule a time with him.

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Final Examination or Evaluation

This course will have a cumulative final exam given during exam week. Per **University schedule (https://www.sjsu.edu/classes/final-exam-schedule/fall-2024.php)** this is on Dec. 15, 2026 from 1-3p.

There will be two in-class exams given in the semester (the last being the final exam).

Grading Information

Determination of Grades

Grades will be calculated based on the individual project grades, the two mid-semester exams, the final, discussion participation. Briefly, the weighted distribution is,

Course Project	40%
Midterm 1	15%
Midterm 2	15%
Final	20%
Homework/Class Participation	10%

The grade distribution will be:

Percentage	**Grade**
93 and above	A
90-93	A-
87-90	B+
84-87	B
80-84	B-

77-80	C+
74-77	C
70-74	C-
67-69	D+
64-67	D
60-64	D-
59 and below	F

Classroom Protocol

This is your class. Please ask questions. Please come prepared. Do not engage in activity that may distract other students.

I do not take attendance except for the first two classes. Students not attending either of the first two classes will be dropped to make room for students on the waiting list. Attempting to get marked as present (by have someone else attend in your place or using technological deceptions) will be considered academic dishonesty and at a minimum will result in you getting dropped from the course.

Course material developed by the instructor is the intellectual property of the instructor. Students ***should not*** publicly share or upload instructor generated material for this course such as exam questions, lecture notes, hands-on exercises or homework solutions without instructor permission.

The schedule listed below is tentative and may change based on student needs. Furthermore, the programming project is new and we will learn by doing :-).

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Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate

Programs' **Syllabus Information web page (http://www.sjsu.edu/gup/syllabusinfo/)** at http://www.sjsu.edu/gup/syllabusinfo/" Make sure to review these policies and resources.

Course Assignments

There are two types of assignments for this course:

1. **Weekly Written Homework:** These will be assigned on Tuesday and will be due before class the following Tuesday. Answers should be submitted on canvas. Late submissions will not be accepted. These will count towards class participation. The work you submit must be your work and your work alone.
2. **Programming Labs:** (More on this below). There will be 5 programming labs and a course project during the semester. You will be writing Verilog programs. Get familiar with the toolchain :).

Programming Labs/Project

This course project builds upon **individual** programming assignments**. Individual programming assignments are not group projects.** The programs you submit must be your work and your work alone.

Caveats:

1. A requirement is that you **do not** publish solutions on public GitHub repos.
2. The labs are known to be demanding and debugging can be time consuming. So, please get started early for each lab.

Early submission:

- Submissions that are at least 2 or more days ***earlier*** than the deadline will get a 10% bonus.

Late Submissions:

1. Submissions that are up to a week late will be penalized 30% of the score.
2. Submissions that are up to two weeks late will be penalized 50% of the score.
3. I will not accept submissions that are more than two weeks beyond the submission date. This will be considered as a non-submission.
4. At my discretion, non-submissions will likely result in a grade penalty.

Cheating/Academic Dishonesty

I take issues of Academic Dishonesty very seriously. ***Do not cheat***. ***Do not share code***. If we detect cheating in a programming assignment or an exam, you will get a **0** for that lab/exam. Repeat

offense will likely lead to a **F** grade in the course.

Artificial intelligence (AI) tools like ChatGPT, Google Gemini, and GitHub Copilot are not permitted to be used as a replacement for the writing or problem-solving components of this class. SJSU's subscription to Gradescope has an AI-detection feature, and assignments that have been determined by that application or by other convincing evidence to have been written by AI in substantial fractions will receive an automatic zero. The incident will also be reported to the University as academic misconduct.

Preparing for the course

Start preparing for the course by doing the tutorials:

- Learn UNIX command line tools: **UNIX Tutorial (https://info-ee.surrey.ac.uk/Teaching/Unix/)**
- Learn C: **C tutorial (https://www.cs.hmc.edu/~rhodes/courses/cs134/sp19/readings/pointers.pdf)**

Course Schedule

(Tentative) Course Schedule

Week	Date	Topic/Theme	Reading(s) from H&P
1	8/20	Overview	1-1.5
2	8/25	Performance: Moore's law, Dennard Scaling, Amdahl's law	1.6-1.8, 1.11 and Moore's law paper
	8/27	Verilog Tutorial, Combinational Circuits	Appendix B.1-B.4
3	9/1	Arithmetic, Adder, In-class activity	• 3.1-3.2 • (On your own: Watch the **video (https://www.youtube.com/playlist?list=PLiwt1iVUib9vXV5xqD_QCTU5SVMjDN5U_)** on Logic Design)
	9/3	MIPS ISA (Part 1), Carry-look ahead adder	2.1-2.5

4	9/8	MIPS ISA (Part 2), Shifter	2.5-2.7, 2.10
	9/10	MIPS ISA (Part 3: Procedures), Sequential Circuits	2.8 and Appendix B (B.7-B.9)
5	9/15	Processor: Single cycle data path	4.1-4.3 and Appendix B (B.7-B.9)
	9/17	Processor: Single cycle control path	4.4 and **Appendix D (https://sjsu.instructure.com/courses/1635878/files/folder/Uploaded%20Med preview=86094578)**
6	9/22	Processor Pipelining	4.6-4.7
	9/24	Processor Pipelining	4.6-4.7
7	9/29	**Midterm-I**	
	10/1	Processor Pipelining	4.6-4.7
8	10/6	Pipeline hazards	4.8-4.9
	10/8	Pipeline hazards	4.8-4.9
9	10/13	Pipeline hazards (wrap up)	4.9
	10/15	Cache Concepts	5.1-5.2
10	10/20	Cache Design	5.3
	10/22	Cache Performance	5.4
11	10/27	Virtual	5.6-5.7

		Memory	
	10/29	Virtual Memory	
12	11/3	**Midterm-II**	
	11/5	Main Memory & ECC	◦ 5.5, 5.11 ◦ **ECC handout (https://sjsu.instructure.com/courses/1635878/files/folder/Uploaded%20I preview=86793362)**
14	11/10	Exceptions	4.10, 5.7
	11/12	Processor (Superscalar)	◦ 4.11 and Appendix A.7 ◦ (Optional) **MIPS R10K paper (http://ece552.ece.wisc.edu/mipsr1000**
15	11/17	Review of Cache Concepts	
	11/19	Parallel Processors	6.1-6.2
16	11/24	Instruction level Parallelism (ILP)	6.3
	11/26	**Thanksgiving break**	No Class
	12/1	Instruction level Parallelism (ILP)	6.4
	12/3		
17	**12/15**	**Final Exam: 1-3p**	In Class