SJSU SAN JOSÉ STATE UNIVERSITY

College of Science · Computer Science

Computer Architecture CS 147

Fall 2026 Section 03 In Person 3 Unit(s) 08/19/2026 to 12/07/2026 Modified 09/01/2026

Contact Information

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Office hours - Monday 6 pm to 7 pm at

https://sjsu.zoom.us/j/81362836527?pwd=Y01Yc3FPY1YxV0dKOHpJSnFoV29jUT09

Course Description and Requisites

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Prerequisite(s): CS 47 or CMPE 70 (with a grade of "C-" or better), Computer Science or Forensic Science: Digital Evidence majors only.
Grading: Letter Graded.

Classroom Protocols

You are welcome to ask questions while the lecture is in progress, just raise your hand.

Discussions, in general, are allowed and encouraged, but not while the lecture is in progress.

You are expected to participate in the recaps/ ungraded quiz in the beginning of each lecture.

The course design does not require any use of electronics like laptop, tablets or cellphones during the lecture, so they are disallowed.

Disturbing/ distracting the lecture or other students in any way while the lecture is in progress is disallowed. You may quietly leave the class for a break and quietly re-enter without asking permission and/ or disturbing the lecture/ class.

Sharing solutions, answers or code is strictly forbidden and will be handled as per the university policy without exceptions.

Report will be graded similar to CS 197/198 rules, i.e. the nominal grade is 90%. Put another way, if you do all as told, i.e. pretty much what the entire class does, that warrants 90% grade. For >90%, you must do stuff that positively distinguishes you from the rest of the class.

Program Information

Diversity Statement - At SJSU, it is important to create a safe learning environment where we can explore, learn, and grow together. We strive to build a diverse, equitable, inclusive culture that values, encourages, and supports students from all backgrounds and experiences.

Course Materials

You may also use the ARM or MIPS versions of the book by same authors. All chapters are nearly identical except Chapter 2- ISA, for which the required details for RISCV are freely available online.

Lecture assignments will be from the textbook, but you will get the complete question and required details without requiring to have the exact same book and edition.

Computer Organization and Design RISC-V Edition: The Hardware Software Interface

Author: Patterson and Hennessy
Publisher: Morgan Kaufmann
Edition: 1
Availability: etext available from SJSU library

etext from SJSU library -

https://csu-sjsu.primo.exlibrisgroup.com/permalink/01CALS_SJO/5k7on1/alma991014110689502919 (https://csu-sjsu.primo.exlibrisgroup.com/permalink/01CALS_SJO/5k7on1/alma991014110689502919)

Course Requirements and Assignments

Course has 5 H/W assignments. You may write and scan or type in a Word document as long as all answers are legible. You will be graded for what is legible. For every question, 50% of the marks are for showing how the answer was obtained and only 50% marks are for the final answer.

All submissions must be in CANVAS.

Late submissions without proof of an exception circumstance are not allowed.

Grading Information

Grade breakup

H/W Assignments (5)	60% (12% each)

Midterm	15%
Final exam	25%

Criteria

Grading criterion (including the lower limit)

>= 96	A+
93 - 96	A
90 - 93	A-
86 - 90	B+
83 - 86	B
80 - 83	B-
76 - 80	C+
73 - 76	C
70 - 73	C-
66 - 70	D+
63 - 66	D
60 - 63	D-
< 60	F

University Policies

Per University Policy S16-9 (PDF) (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on the Syllabus Information (https://www.sjsu.edu/curriculum/courses/syllabus-info.php) web page. Make sure to visit this page to review and be aware of these university policies and resources.

Course Schedule

Below is a "tentative" schedule. We will follow this by default, but depending on how the class finds some topics, we may choose to spend more or less time on certain topics.

	Chapter 1 Performance & Benchmarks	
	Chapter 2 ISA	HW 1 due
	Chapter 4 Micro-architecture	HW 2 due
	Chapter 5 Memory Hierarchy	
	Mid term (Report submission)	
	Chapter 5 Memory Hierarchy	H/W 3 due
	Chapter 6 Parallel computers	HW 4 due
		HW 5 due
	Final Exam (Presentation)	Dec 15 10:45 am to 12:45 pm